AMENDED CLAIMS:

This listing of claims will replace all prior claim listings in this application.

Listing of Claims:

1. (Currently amended) A semiconductor component comprising:

a semiconductor substrate having an insulating layer on the semiconductor substrate surface and having a capacitance structure in the insulating layer, wherein the capacitance structure comprises:

a first substructure ~~which has~~ having a first cohesive latticed metal region including crossing metal leads, the first substructure ~~which extends~~ extending in a first common plane parallel to the substrate surface such that ~~it~~ the first substructure has common top and bottom surfaces which limit the first cohesive latticed metal region ~~in each of its subregions~~ from above and from below,

wherein the first cohesive latticed metal region is electrically connected to a first connecting line; and

at least two electrically conductive regions in the first substructure and electrically isolated from the crossing metal leads and arranged in openings in the first cohesive latticed metal region ~~of the first substructure~~ at a distance from edge regions of the openings in the first common plane,

wherein the crossing metal leads have a width less than or equal to the distance between the edge regions of the openings and the electrically conductive regions and,

wherein the at least two electrically conductive regions are electrically connected to ~~a~~ second connecting lines, and

wherein the at least two electrically conductive regions comprise one of metal plates or node points between via connections and are electrically isolated from one another by the latticed metal region.

2. (Currently amended) The semiconductor component as claimed in claim 1, wherein the capacitance structure further comprises:

a second substructure parallel to and at a distance from the first substructure wherein the second substructure comprises:

a second cohesive latticed metal region including crossing metal leads which extends in a second common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the second latticed metal region in each ~~of its subregions~~ from above and below; and

electrically conductive regions,

wherein the first and second substructures are electrically connected by the first and second connecting lines.

3. (Currently amended) The semiconductor component as claimed in claim 2, wherein the second substructure is of substantially the same design as the first substructure, and the first and second substructures are laterally offset from one another such that the at least two electrically conductive regions of the first substructure are substantially vertically aligned above crossing points of the metal leads in the second cohesive latticed metal region of the second substructure, and crossing points of the metal leads in the first cohesive latticed metal region of the first substructure are substantially vertically aligned above the electrically conductive regions of the second substructure.

4. (Currently amended) The semiconductor component as claimed in claim 3, wherein the crossing points of the metal leads in the first cohesive latticed metal region of the first substructure are electrically connected to the electrically conductive regions of the second substructure and the at least two electrically conductive regions of the first substructure are electrically connected to the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure by means of at least one respective via connection.

5. (Currently amended) The semiconductor component as claimed in claim 2, wherein the second cohesive latticed metal region of the second substructure is laterally offset from the first substructure, so that the at least two electrically conductive regions of the first substructure are substantially vertically aligned above the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure.

6. (Currently amended) The semiconductor component as claimed in claim 5, wherein the at least two electrically conductive regions of the first substructure and the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure are electrically connected by means of one or more respective via connections.

7. (Previously presented) The semiconductor component as claimed in claim 3 further comprising a metal plate electrically connected to one of the crossing points of the metal leads in the cohesive latticed metal region of the first substructure and to the electrically conductive regions of the second substructure by means of one or more respective via connections.

8. (Previously presented) The semiconductor component as claimed in claim 1, wherein the first cohesive latticed metal region has at least two square or round openings.

9. (Previously presented) The semiconductor component as claimed in claim 1, wherein the first and second connecting lines are at different electrical potentials.

10. (Currently amended) The semiconductor component as claimed in claim 1, wherein a first non-parasitic capacitance exists between the crossing metal leads of

the cohesive latticed metal region and the at least two electrically conductive regions of the first substructure and a second non-parasitic capacitance exists between the first and second connecting lines, and wherein the magnitude of the first non-parasitic capacitance differs from the magnitude of the second non-parasitic capacitance.

11. (Currently amended) A semiconductor component having an integrated capacitance structure, the component comprising:

a semiconductor substrate having a surface;

an insulating layer overlying the surface of the semiconductor substrate;

a capacitance structure in the insulating layer, wherein the capacitance structure comprises:

a first metal lattice including intersecting metal leads in a first common plane parallel to the substrate surface;

a second metal lattice including intersecting metal leads in a second common plane parallel to the substrate surface,

electrically conductive regions arranged in each of at least two openings in each of the first and second metal lattices and electrically isolated from the intersecting metal leads, the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer and electrically isolated from one another by the intersecting metal leads,

wherein the intersecting metal leads have a width less than or equal to a distance between an edge of the openings and the electrically conductive regions; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice are substantially vertically above crossing points of the second metal lattice, and crossing points of the first metal lattice are substantially vertically above the electrically conductive regions of the second metal lattice; and

first and second electrical connections between the first and second lattices such that the first and second electrical connections are at different electrical potential.

12. (Currently amended) The semiconductor component as claimed in claim 11, wherein the electrically conductive regions of the first and second metal lattices comprise metal plates or node points.

13. (Previously presented) The semiconductor component as claimed in claim 11, wherein the electrical connections comprise:

first connecting lines electrically connecting the electrically conductive regions of the first metal lattice to crossing points of the intersecting metal leads of the second metal lattice; and

second connecting lines electrically connecting crossing points of the intersecting metal leads of the first metal lattice to the electrically conductive regions of the second metal lattice.

14. (Previously presented) The semiconductor component as claimed in claim 11 further comprising a metal plate in a third common plane parallel to the substrate surface and electrically coupled to the first and second metal lattices by the first and second electrical connections.

15. (Previously presented) The semiconductor component as claimed in claim 11 further comprising a third metal lattice including intersecting metal leads in a third common plane parallel to the substrate surface, wherein the intersecting metal leads define openings, wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the first and second metal lattices by the electrical connections.

16. (Currently amended) A semiconductor component having an integrated capacitance structure, the capacitance structure comprising:

an insulating layer;

a first metal lattice in the insulating layer, the first metal lattice including intersecting metal leads in a first common plane and defining a checkerboard pattern;

a second metal lattice in the insulating layer, the second metal lattice including intersecting metal leads in a second common plane~~,~~ and defining a checkerboard pattern;

electrically conductive regions electrically isolated from the crossing metal leads and arranged in openings in at least one of the first and second metal lattices, the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer and electrically isolated from one another by the intersecting metal leads,

wherein the intersecting metal leads have a width less than or equal to the distance between the edge regions of the openings and the electrically conductive regions; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice are substantially vertically above crossing points of the second metal lattice, and crossing points of the first metal lattice are substantially vertically above the electrically conductive regions of the second metal lattice;

a third metal structure in the insulating layer in a third common plane the third metal structure comprising one of a third metal lattice or a metal plate; and

first and second electrical connections between the first and second lattices and the third metal structure, such that the first and second electrical connections are at different electrical potential.

17. (Previously presented) The semiconductor component as claimed in claim 16, wherein the third metal structure comprises a metal plate electrically coupled to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections.

18. (Previously presented) The semiconductor component as claimed in claim 16, wherein the third metal structure comprises a third metal lattice including intersecting metal leads, wherein the intersecting metal leads define openings, wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections.

19. (Previously presented) The semiconductor component as claimed in claim 16, wherein the first electrical connection electrically connect the electrically conductive regions of the first metal lattice to the crossing points of the second metal lattice, and wherein the second electrical connection electrically connect the crossing points of the first metal lattice to the electrically conductive regions of the second metal lattice.

20. (Previously presented) The semiconductor component as claimed in claim 16, wherein the third metal structure comprises a third metal lattice including intersecting metal leads and electrically conductive regions in openings defined by the intersecting metal leads.

21. (Previously presented) The semiconductor component as claimed in claim 20, wherein non-parasitic capacitances exist between the electrically conductive regions and intersecting metal leads in the first, second, and third metal lattices and wherein non-parasitic capacitances exist between the first and second connecting lines.

22. (New) A semiconductor capacitance component comprising:

a first metal lattice extending in a plane and including crossing metal leads that define crossing points and a plurality of openings therein, where each of the plurality of openings are circumferentially enclosed by the crossing metal leads;

first connecting lines electrically connected to the first metal lattice;

first electrically conductive regions comprising one of metal plates or node points between via connections in the plurality of openings in the first metal lattice and electrically isolated from the crossing metal leads; and

second connecting lines electrically connected to the first electrically conductive regions and electrically isolated from one another by the first metal lattice.

23. (New) The semiconductor component as claimed in claim 22 further comprising:

a second metal lattice extending in a second plane and including crossing metal leads that define crossing points and a plurality of openings therein, where each of the plurality of openings are circumferentially bounded by the crossing metal leads; and

second electrically conductive regions in the plurality of openings of the second metal lattice and substantially vertically aligned with the crossing points of the first metal lattice,

wherein the first connecting lines electrically connect the crossing points of the first metal lattice to the second electrically conductive regions, and

the second connecting lines electrically connect the first electrically conductive regions to the crossing points of the second metal lattice.